NOORUL ISLAM CENTRE FOR HIGHER EDUCATION

(Deemed to be University Under Section 3 of the UGC Act, 1956)
Kumaracoil, Thuckalay

DEPARTMENT OF

ELECTRICAL AND ELECTRONICS ENGINEERING

M.E. APPLIED ELECTRONICS

CURRICULUM AND SYLLABI

REGULATION 2021

NOORUL ISLAM CENTRE FOR HIGHER EDUCATION
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Regulation : 2021

Curriculum and Syllabi

M.E Programme
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

M.E – APPLIED ELECTRONICS

Vision of the University
To be recognized by the Government and society at large as an institution able to deliver excellence with relevance in the field of higher education and research focusing on the needs of the nation in tune with the technological revolution to cope with the knowledge explosion and global competence.

Mission of the University
To develop the institution as a Centre of Excellence, keeping pace with the advances in the field, so as to provide quality higher education to the students and instill in them high standards of discipline and ethics so that they become enlightened individuals in the service of humanity and to carry out focused research in the frontier areas of science and technology.

Faculty of Electrical Engineering

Department of Electrical and Electronics Engineering

Vision of the Department
To evolve into a nationally recognized department in the frontier areas of Electrical and Electronics Engineering and to be recognized by the government and society at large and by the industry and commerce in particular as an institution able to deliver excellence with relevance in the field of technical education focusing on the needs of the nation in tune with the technological revolution.

Mission of the Department
To produce Electrical and Electronics Engineering graduates having professional excellence, to provide technical support to budding entrepreneurs and existing industry and to Develop the institution as a centre of Excellence , keeping pace with advances in the field, so as to provide quality higher Education to the students and instill in them high standards of discipline and ethics so that they become enlightened individuals in the service of humanity and to carry out focused research in the frontier areas of science and technology.

Programme Educational Objectives - PEO	
PEO-01	The engineers of Applied Electronics, design circuits and develop systems in contemporary and frontier areas of electronics.
PEO-02	The enhanced skills of the engineers meet the demands and expectations of automation in various industries.
PEO-03	The graduates with professional competency promote and support creative research and developmental activities.

Graduate	
GA-1	**Advanced Engineering Expertise** Master advanced engineering principles and apply them to design, analyze, and innovate systems that address both present and emerging global challenges across diverse industries.
GA-2	**Leadership in Research and Innovation** Lead groundbreaking research and foster innovation by identifying opportunities for technological advancements, contributing original ideas that push the boundaries of engineering knowledge.
GA-3	**Sustainable Engineering Practices** Develop and implement engineering solutions that integrate sustainability, environmental stewardship, and resource efficiency, ensuring the long-term impact and responsibility of all projects.
GA-4	**Ethical and Strategic Decision-Making** Make informed, ethical decisions in complex engineering contexts, considering societal needs, environmental implications, and the long-term consequences of engineering practices.
GA-5	**Global Competence in Engineering Solutions** Exhibit a deep understanding of global engineering standards and practices, addressing international challenges and cultural sensitivities in engineering projects to make a broader societal impact.
GA-6	**Technological Agility and Lifelong Learning** Stay ahead of technological trends and exhibit agility in learning new tools, methodologies, and technologies, ensuring continuous professional growth in a rapidly evolving engineering landscape.
GA-7	**Interdisciplinary and Collaborative Innovation** Excel in multidisciplinary collaborations, leveraging knowledge from multiple fields to solve complex, large-scale engineering problems that require comprehensive and innovative solutions.
GA-8	**Data-Driven Decision Making** Employ advanced data analytics, machine learning, and computational tools to derive insights and make informed engineering decisions that improve
GA-9	**Entrepreneurial Mindset and Innovation Leadership** Cultivate an entrepreneurial mindset, translating engineering innovations into viable products, solutions, or services, and leading teams toward commercialization and societal impact.
GA-10	**Safety, Risk, and Crisis Management** Implement and manage advanced safety protocols and risk mitigation strategies to protect individuals, communities, and ecosystems in engineering practices, particularly in high-stakes and crisis environments.

Programme Outcome - PO	
PO-A	An ability to integrate knowledge from the fields of study and arrive solutions for complex engineering tasks.
PO-B	An ability to understand different kinds of problem solving methods through the imparted domain knowledge.
PO-C	To solve a broad research competence problem systematically, to analyze the reasonable value of new ideas and technology decisions with confidence.
P0-D	An ability to empower with an in-depth understanding of research orientation in their chosen domain with a strategy.
PO-E	An ability to design an ICT based system for optimal analysis of systems.
PO-F	An ability to stimulate opportunities to contribute skills thereby providing an option to find applications suiting the revolutionized concepts.
PO-G	To research and implement a project that meets the needs within realistic constraints.
PO-H	To inculcate a desire for continuous learning and creativity, with emerging tools and technology.
PO-I	An ability to understand the responsibility of taking professional decisions based on the impact of socio- economic issues.
PO-J	To develop the self-confidence towards the professional competency with interpersonal skills.
PO-K	To develop a skill in conducting research in their chosen field, and present their results and findings in scientific forums.
PO-L	An ability to deliver inspiring thoughts and show unparalleled commitment.

Mapping of Graduate Attributes and Programme Educational Objectives

GAs / PEOs	GA-01	GA-02	GA-03	GA-04	GA-05	GA-06	GA-07	GA-08	GA-09	GA-10
PEO-1	H	A	A	A	A	A	A	A	A	A
PEO-2	A	H	H	A	A	A	A	A	A	A
PEO-3	A	A	A	H	H	A	A	A	A	A

H- Highly Associated A- Associated Not – Not Associated

Mapping of Graduate Attributes and Programme Outcomes (PO)

GAs / POs	GA-01	GA-02	GA-03	GA-04	GA-05	GA-06	GA-07	GA-08	GA-09	GA-10
PO-A	H	H	A	A	A	A	H	Not	H	Not
PO-B	H	H	A	A	A	A	H	Not	H	Not
PO-C	H	H	H	H	H	A	H	Not	H	Not
P0-D	H	H	A	A	H	H	H	Not	A	Not
PO-E	A	A	A	A	A	H	A	Not	A	Not
PO-F	Not	H	A	A	A	A	H	H	Not	H
PO-G	H	H	H	H	A	H	A	H	Not	H
PO-H	A	H	H	H	H	H	A	H	Not	H
PO-I	A	A	A	A	H	H	H	H	A	H
PO-J	Not	Not	Not	Not	Not	H	H	H	Not	H
PO-K	H	A	H	H	H	H	H	H	H	A
PO-L	H	A	A	A	H	H	H	H	H	A

H- Highly Associated A- Associated Not – Not Associated

Mapping of Programme Educational Objective (PEOs) and Programme Outcomes (POs)

PEO / PO	PEO-01	PEO-02	PEO-03
PO-A	H	A	A
PO-B	A	H	A
PO-C	A	A	H
P0-D	A	A	H
PO-E	A	H	A
PO-F	A	H	A
PO-G	A	H	A
PO-H	A	A	H
PO-I	A	H	H
PO-J	A	A	H
PO-K	H	A	H
PO-L	A	H	A

H- Highly Associated A- Associated Not – Not Associated

Duration of the Programme: 2 Years/ 4 Semesters

Total credit: 67

CURRICULUM & SYLLABUS

SEMESTER I

SI. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	MA3501	Advanced Mathematics	3	1	0	4
2.	EE3501	Advanced Digital Signal Processing	3	0	0	3
3.	EE3502	Advanced Computer Architecture	3	0	0	3
4.	EE3503	Advanced Microprocessor and Microcontroller	3	0	0	3
5.	EExxx1	Elective-I	3	0	0	3
6.	EExxx2	Elective – II	3	0	0	3
PRACTICAL						
7.	EE3571	Electronic Design Laboratory – I	0	0	2	1
Total			**18**	**1**	**2**	**20**

SEMESTER II

SI. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	EE3504	Analysis and Design of Analog Integrated Circuits	3	0	0	3
2.	EE3505	Machine Learning	3	0	0	3
3.	EE3506	Digital Control Engineering	3	0	0	3
4.	EE3507	Advanced Embedded Systems	3	0	0	3
5.	EExxx3	Elective-III	3	0	0	3
6.	EExxx4	Elective- IV	3	0	0	3
PRACTICAL						
7.	EE3572	Electronic Design Laboratory – II	0	0	2	1
Total			**18**	**0**	**2**	**19**

SEMESTER III

SI. NO.	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	EExxx5	Elective- V	3	0	0	3
2.	OE-I	Open Elective-I	3	0	0	3
PRACTICAL						
3.	EE35P1	Project Work - Phase I	0	0	18	6
TOTAL			**6**	**0**	**18**	**12**

SEMESTER IV

SI. NO.	COURSE CODE	COURSE TITLE	L	T	P	C
PRACTICAL						
1.	EE35P2	Project Work - Phase II	**0**	**0**	**32**	**16**

Total Credits: 67

LIST OF PROGRAM ELECTIVES

SI. NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1.	EE35A1	Robotics	3	0	0	3
2.	EE35A2	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
3.	EE35A3	Low Power VLSI	3	0	0	3
4.	EE35A4	Internet Working and Multimedia	3	0	0	3
5.	EE35A5	DSP Integrated Circuits	3	0	0	3
6.	EE35A6	High Speed Switching Architecture	3	0	0	3
7.	EE35A7	CADD for VLSI Circuits	3	0	0	3
8.	EE35A8	Data Converters	3	0	0	3
9.	EE35A9	Advanced Digital system design	3	0	0	3
10.	EE35B1	Digital Image Processing and Applications	3	0	0	3
11.	EE35B2	VLSI Design	3	0	0	3
12.	EE35B3	High Performance Communication Networks	3	0	0	3
13.	EE35B4	Embedded Analog Interfacing	3	0	0	3

LIST OF OPEN ELECTIVES

SI. NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1.	EC35B1	Fundamental of Soft Computing Techniques	3	0	0	3
2.	GE35A1	Business Analytics	3	0	0	3
3.	GE35A2	Industrial Safety	3	0	0	3
4.	GE35A3	Operations Research	3	0	0	3
5.	GE35A4	Cost Management of Engineering Projects	3	0	0	3
6.	GE35A5	Composite Materials	3	0	0	3
7.	GE35A6	Waste to Energy	3	0	0	3

SEMESTER-I

SI. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	MA3501	Advanced Mathematics	3	1	0	4
2.	EE3501	Advanced Digital Signal Processing	3	0	0	3
3.	EE3502	Advanced Computer Architecture	3	0	0	3
4.	EE3503	Advanced Microprocessor and Microcontroller	3	0	0	3
5.	EExxx1	Elective-I	3	0	0	3
6.	EExxx2	Elective – II	3	0	0	3
PRACTICAL						
7.	EE3571	Electronic Design Laboratory – I	0	0	2	1
Total			**18**	**1**	**2**	**20**

MA3501	ADVANCED MATHEMATICS	L	T	P	C
		3	**1**	**0**	**4**

AIM:

To gain a well-found knowledge of optimizing a function and variation problems which provide necessary mathematical support and confidence to tackle real life problems.

OBJECTIVES:

The course objective is, the students will be able to apply various methods in Linear Algebra to solve the system of linear equations, use two-dimensional random variables, and correlations in solving application problems apply the ideas of Random Processes and understand the basic characteristic features of a queueing system and acquire skills in analyzing queueing models.

UNITI LINEAR ALGEBRA **9**

Vector spaces – Norms – Inner products – Eigenvalues using QR transformations —Generalized eigenvectors – Jordan Canonical forms – Singular value decomposition and applications – Pseudo inverse

UNIT II LINEAR PROGRAMMING **9**

Formulation – Graphical solution – Simplex method: Big M Method– Transportation problems– Assignment models

UNIT III PROBABILITY AND RANDOM VARIABLES **9**

Probability Concepts – Axioms of probability – Conditional probability – Random variables

– Probability functions – Two-dimensional random variables – Joint distributions – Marginal and conditional distributions – Correlation.

UNIT IV RANDOM PROCESSES **9**

Classification – Stationary random processes – Ergodic process - The autocorrelation – CrossCorrelations – Properties - Power spectral density, Cross Power spectral density.

UNIT V QUEUING THEORY **9**

Birth and Death process - Markovian queuing models – Little's formulae - M/M/1,M/M/C finite and infinite capacity (steady state solutions only**)**

L: 45 + T: 15, TOTAL: 60 PERIODS

REFERENCES:

1. Friedberg A.H, Insel A.J. and Spence L, "Linear Algebra", Prentice Hall of India, New Delhi, 2004.
2. Taha, H.A., "Operations Research – An Introduction", Sixth Edition, Prentice-Hall of India, New Delhi.
3. Gupta, P.K. and Hira, D.S., "Operations Research", S.Chand& Co. New Delhi.
4. Peebles Jr., P.Z., "Probability, Random Variables and Random Signal Principles" ,McGraw-Hill Inc.
5. Gross, D., Shortie, J.F., Thompson, J.M and Harris, C.M., "Fundamentals of Queueing Theory", 4th Edition, Wiley,2014.

EE3501	ADVANCED DIGITAL SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

AIM

To introduce the students the various concepts and techniques used in advanced digital signal processing techniques.

OBJECTIVES

- To study the parametric methods for power spectrum estimation.
- To study adaptive filtering techniques using lms algorithm and to study the applications of adaptive filtering.
- To study multirate signal processing fundamentals.
- To study the analysis of speech signals.

Subject Code: EE3501 Subject Name: Advanced Digital Signal Processing		
Course Outcome – Cos		**Cognitive Skill**
CO-01	Able to understand the parametric methods of power estimation	U
CO-02	Able to perform analyses of speech signals	An

CO-03	Able to do multi-rate signal processing	A
CO-04	Able to analyze the adaptive filtering techniques	An
CO-05	Able to remember the wavelet transforms	R

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	S	S	M	S	M	S	S	M	S	L	L
CO-02	S	M	S	S	M	S	S	S	S	S	L	L
CO-03	S	M	M	S	S	S	S	S	S	M	S	L
CO-04	M	S	M	M	M	M	S	M	S	L	L	M
CO-05	M	S	S	S	M	S	M	S	S	M	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I **9**

DISCRETE RANDOM SIGNAL PROCESSING

Discrete Random Processes- Ensemble averages, stationary processes, Autocorrelation and Auto covariance matrices. Parseval's Theorem, Wiener-Khintchine Relation- Power Spectral Density- Periodogram Spectral Factorization, Filtering random processes. Low Pass Filtering of White Noise. Parameter estimation: Bias and consistency.

UNIT II **9**

SPECTRUM ESTIMATION

Estimation of spectra from finite duration signals, Non-Parametric Methods-Correlation Method , Periodogram Estimator, Performance Analysis of Estimators -Unbiased, Consistent Estimators- Modified periodogram, Bartlett and Welch methods, Blackman –Tukey method. Parametric Methods - AR, MA, ARMA model based spectral estimation. Parameter Estimation -Yule-Walker equations, solutions using Durbin’s algorithm

UNIT III **9**

WIENER FILTERS AND LINEAR PREDICTION

Linear prediction- Forward and backward predictions, Solutions of the Normal equations- Levinson-Durbin algorithms. Least mean squared error criterion -Wiener filter for filtering and prediction , FIR Wiener filter and Wiener IIR filters ,Discrete Kalman filter

UNIT IV **9**

ADAPTIVE FILTERS

FIR adaptive filters -adaptive filter based on steepest descent method-Widrow-Hoff LMS adaptive algorithm, Normalized LMS. Adaptive channel equalization-Adaptive echo cancellation-Adaptive noise cancellation- Adaptive recursive filters (IIR). RLS adaptive filters-Exponentially weighted RLS-sliding window RLS.

UNIT V **9**

MULTIRATE DIGITAL SIGNAL PROCESSING

Mathematical description of change of sampling rate - Interpolation and Decimation , Decimation by an integer factor - Interpolation by an integer factor, Sampling rate conversion by a rational factor, Filter implementation for sampling rate conversion- direct form FIR structures, Polyphase filter structures, time-variant structures. Multistage implementation of multirate system. Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

TOTAL: 45 PERIODS

REFERENCES:

1.Monson H.Hayes, Statistical Digital Signal Processing and Modeling, John Wiley and Sons, Inc.,Singapore, 2002.

2.John G. Proakis, Dimitris G.Manolakis, Digital Signal Processing Pearson Education, 2002.

3.John G. Proakis et.al.,'Algorithms for Statistical Signal Processing', Pearson Education, 2002.

4.Dimitris G.Manolakis et.al.,'Statistical and adaptive signal Processing', McGraw Hill, Newyork,2000.

5.Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.(For Wavelet Transform Topic.

EE3502	ADVANCED COMPUTER ARCHITECTURE	L	T	P	C
		3	0	0	3

AIM

To expose to the recent trends and different types of multicore architectures.

OBJECTIVES

- To introduce the students to the recent trends in the field of Computer Architecture and identify performance related parameters.
- To learn the different multiprocessor issues.
- To expose the different types of multicore architectures.
- To understand the design of the memory hierarchy.

Subject Code:EE3502	**Subject Name: Advanced Computer Architecture**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Identify the limitations of ILP.	R, U
CO-02	Discuss the issues related to multiprocessing and suggest solutions	An
CO-03	Discuss the various techniques used for optimising the cache performance	E
CO-04	Point out the salient features of different multicore architectures and how they exploit parallelism.	U, An
CO-05	Design hierarchal memory system and Point out how data level parallelism is exploited in architectures	A

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	S	S	M	S	M	S	S	M	S	L	L
CO-02	S	M	S	S	M	S	S	S	S	S	L	L
CO-03	S	M	M	S	S	S	S	S	S	M	S	L
CO-04	M	S	M	M	M	M	S	M	S	L	L	M
CO-05	M	S	S	S	M	S	M	S	S	M	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I FUNDAMENTALS OF COMPUTER DESIGN AND ILP 9

Fundamentals of Computer Design – Measuring and Reporting Performance – Instruction Level Parallelism and its Exploitation – Concepts and Challenges –Exposing ILP - Advanced Branch Prediction - Dynamic Scheduling - Hardware-Based Speculation - Exploiting ILP - Instruction Delivery and Speculation - Limitations of ILP - Multithreading

UNIT II MEMORY HIERARCHY DESIGN 9

Introduction – Optimizations of Cache Performance – Memory Technology and Optimizations – Protection: Virtual Memory and Virtual Machines – Design of Memory Hierarchies – Case Studies.

UNIT III MULTIPROCESSOR ISSUES 9

Introduction- Centralized, Symmetric and Distributed Shared Memory Architectures –Cache Coherence Issues – Performance Issues – Synchronization – Models of Memory Consistency – Case Study- Interconnection Networks – Buses, Crossbar and Multi-stage Interconnection Networks

UNIT IV MULTICORE ARCHITECTURES 9

Homogeneous and Heterogeneous Multi-core Architectures – Intel Multicore Architectures – SUN CMP architecture – IBM Cell Architecture. Introduction to Warehouse-scale computers Architectures- Physical Infrastructure and Costs- Cloud Computing –Case Study- Google Warehouse-Scale Computer.

UNIT V VECTOR, SIMD AND GPU ARCHITECTURES 9

Introduction-Vector Architecture – SIMD Extensions for Multimedia – Graphics Processing Units – Case Studies – GPGPU Computing – Detecting and Enhancing Loop Level Parallelism-Case Studies.

TOTAL :45 PERIODS

REFERENCES

1.Darryl Gove, ―Multicore Application Programming: For Windows, Linux, and Oracle Solaris‖, Pearson, 2011

2.David B. Kirk, Wen-mei W. Hwu, ―Programming Massively Parallel Processors‖, Morgan Kauffman, 2010

3.David E. Culler, Jaswinder Pal Singh, ―Parallel computing architecture : A hardware/software approach‖ , Morgan Kaufmann /Elsevier Publishers, 1999

4.John L. Hennessey and David A. Patterson, ―Computer Architecture – A Quantitative Approach‖, Morgan Kaufmann / Elsevier, 5th edition, 2012.

5.Kai Hwang and Zhi.WeiXu, ―Scalable Parallel Computing‖, Tata McGraw Hill, NewDelhi, 2003

EE3503	**ADVANCED MICROPROCESSOR AND MICRO CONTROLLERS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

PREREQUISITE: Microprocessor and micro controllers.

AIM

To do an advanced study of microprocessor, Pentium, ARM architectures and MOTOROLA 68HC11 and PIC micro controller architecture.

OBJECTIVES

- To do a detailed study of microprocessor architecture.
- To study the Pentium processor in detail.
- To study the ARM processor in detail.
- To do the detailed study of MOTOROLA 68HC11 micro controller.
  To do the detailed study of PIC micro controller.

Subject Code:: **EE3503 Subject Name: Advanced Microprocessors and micro controllers**		
Course Outcome – Cos		**Cognitive Skill**
CO-01	To understand about the microprocessor architecture and its applications	U,A
CO-02	To analyze about the performance of CISE ARCHETECTURE	An
CO-03	To remember the operations of ARM architecture	R
CO-04	To understand about the working of MOTOROLA micro controllers	U
CO-05	To understand the working and applications of PIC microcontrollers	U,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO – I	PO-J	PO- k	PO -L
CO-01	S	L	N	S	N	S	S	N	N	N	S	N
CO-02	S	N	M	S	N	L	S	N	N	N	M	N
CO-03	L	S	M	L	N	S	L	N	L	N	S	N
CO-04	S	L	N	L	N	S	S	N	N	N	L	N
CO-05	L	N	N	L	N	S	S	N	N	N	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I **9**

MICROPROCESSOR ARCHITECTURE

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC..

UNIT II **9**

HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III **9**

HIGH PERFORMANCE RISC ARCHITECTURE: ARM

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV **9**

MOTOROLA 68HC11 MICROCONTROLLERS

Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V **9**

PIC MICRO CONTROLLER

CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter – PWM and introduction to C-Compilers.

TOTAL: 45 PERIODS

REFERENCES:

1.Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995

2.James L. Antonakos, “The Pentium Microprocessor ‘’ Pearson Education, 1997.

3.Steve Furber, ‘’ ARM System –On –Chip architecture “Addison Wesley, 2000.

4.Gene .H.Miller.” Micro Computer Engineering,” Pearson Education, 2003.

5.John .B.Peatman, “Design with PIC Microcontroller, Prentice hall, 1997.

6.James L.Antonakos,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.

7.Barry.B.Breg,” The Intel Microprocessors Architecture , Programming and Interfacing “, PHI, 2002.

8.Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprints 2001..

Readings: Web links www.ocw.nit.edu www.arm.com

EE3571	ELECTRONIC DESIGN LABORATORY – I	L	T	P	C
		0	0	2	1

AIM:

To design systems using PIC microcontrollers, DSP processor, FPGA and to design digital systems using VHDL and Verilog.

OBJECTIVES:

- To design systems using PIC microcontroller
- To implement adaptive filters, periodogram and multistage multirate system in DSP processor
- To model sequential digital system using VHDL & Verilog
- To design ALU using FPGA and to design systems using 16 -bit Microprocessors

Subject Code:EE3571	**Subject Name: Electronic Design Laboratory - I**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Analyze and design systems using PIC microcontroller	An
CO-02	Analyze performance adaptive filters, periodogram and multistage multirate system in DSP processor	An
CO-03	Understand the VHDL language and apply it to the sequential circuits	A
CO-04	Understand the Verilog HDL language and apply it to the sequential circuits	U

CO-05	Design and analyse the performance of ALU using FPGA	An

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	S	S	M	M	N	L	L	S	S	S	S
CO-02	S	S	S	M	M	N	L	L	S	S	S	S
CO-03	M	S	L	M	L	N	L	M	S	M	S	L
CO-04	M	S	L	M	L	N	L	M	S	M	S	L
CO-05	S	S	S	M	M	N	L	L	S	S	S	S

S- Strong, M- Medium, L-Low, N- Not Relevant

1.System design using PIC Microcontroller.

2.Implementation of Adaptive Filters, periodogram and multistage multirate system in DSP Processor

3.Simulation of QMF using Simulation Packages

4.Modeling of Sequential Digital system using VHDL.

5.Modeling of Sequential Digital system using Verilog.

6.Design and Implementation of ALU using FPGA.

7.Simulation of NMOS and CMOS circuits using SPICE.

8.System design using 16- bit Microprocessor.

TOTAL: 45 PERIODS

OUTCOMES:

1. To design PIC microcontroller and filters.
2. Understand the VHDL language to implement in sequential circuits.
3. The performance of ALU and FPGA can be studied and analyzed.

SEMESTER-II

SI. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	EE3504	Analysis and Design of Analog	3	0	0	3

		Integrated Circuits				
2.	EE3505	Machine Learning	3	0	0	3
3.	EE3506	Digital Control Engineering	3	0	0	3
4.	EE3507	Advanced Embedded Systems	3	0	0	3
5.	EExxx3	Elective-III	3	0	0	3
6.	EExxx4	Elective- IV	3	0	0	3
PRACTICAL						
7.	EE3572	Electronic Design Laboratory – II	0	0	2	1
Total			**18**	**0**	**2**	**19**

EE3504	**ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

AIM

To do an advanced study of analysis and design of integrated circuits, operational amplifiers and multipliers.

OBJECTIVES:

- To design the single stage amplifiers using pmos and nmos driver circuits with different loads.
- To analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
- To study the different types of current mirrors and to know the concepts of voltage and current reference circuits.

Subject Code: **EE3504** Subject Name: Analysis and Design of Analog Integrated Circuit*s*		
Course Outcome – Cos		**Cognitive Skill**
CO-01	To understand about MOS devices	R
CO-02	Analyze of difference amplifiers with active load	An
CO-03	Analyze of operational amplifiers circuit	An
CO-04	Analyze four quadrant multiplier	An
CO-05	To understand about different MOS technology	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / **CO**	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO- J	PO- k	PO –L

CO-01	S	S	S	S	M	S	S	M	N	N	S	N
CO-02	S	S	M	M	M	L	S	M	N	N	M	N
CO-03	S	S	S	M	M	M	L	M	N	N	S	N
CO-04	S	S	M	S	S	M	S	M	N	N	M	N
CO-05	S	S	M	S	L	S	S	M	N	N	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I SINGLE STAGE AMPLIFIERS **9**

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads

UNIT II FREQUENCY RESPONSE AND NOISE ANALYSIS **9**

Miller effect, Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III OPERATIONAL AMPLIFIERS **9**

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION **9**

General considerations, Multipole systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, and Other compensation techniques.

UNIT V BIASING CIRCUITS **9**

Basic current mirrors, cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL:45 PERIODS

.**REFERENCES:**

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2001
3. Willey M.C. Sansen, “Analog design essentials”, Springer, 2006.
4. Grebene, “Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons,Inc., 2003.
5. Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Second edition, Oxford University Press, 2002

EE3505	**MACHINE LEARNING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

AIM

To explore the basics of machine learning for problem solving.

OBJECTIVES

- To understand the need for machine learning for various problem solving
- To study the various supervised, semi-supervised and unsupervised learning algorithms in machine learning
- To understand the latest trends in machine learning
- To design appropriate machine learning algorithms for problem solving

Subject Code: **EE3505** Subject Name: Problem solving and Python programming		
Course Outcome – Cos		**Cognitive Skill**
CO-01	Learning problems, perspectives and Issues	R, U
CO-02	Ability to understand neural networks and genetic algorithm models of evaluation.	A
CO-03	Understand Bayesian learning	U, An
CO-04	Evaluate and define instant based learning	E
CO-05	Study the rules and regulations of advanced learning	A

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO- J	PO-k	PO-L
CO-01	S	S	S	M	S	M	S	S	M	S	L	L
CO-02	S	M	S	S	M	S	S	S	S	S	L	L
CO-03	S	M	M	S	S	S	S	S	S	M	S	L
CO-04	M	S	M	M	M	M	S	M	S	L	L	M
CO-05	M	S	S	S	M	S	M	S	S	M	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I INTRODUCTION **9**

Learning Problems – Perspectives and Issues – Concept Learning – Version Spaces and Candidate Eliminations – Inductive bias – Decision Tree learning – Representation – Algorithm – Heuristic Space Search.

UNIT II NEURAL NETWORKS AND GENETIC ALGORITHMS **9**

Neural Network Representation – Problems – Perceptron – Multilayer Networks and Back Propagation Algorithms – Advanced Topics – Genetic Algorithms – Hypothesis Space Search – Genetic Programming – Models of Evaluation and Learning.

UNIT III BAYESIAN AND COMPUTATIONAL LEARNING **9**

Bayes Theorem – Concept Learning – Maximum Likelihood – Minimum Description Length Principle – Bayes Optimal Classifier – Gibbs Algorithm – Naïve Bayes Classifier – Bayesian Belief

Network – EM Algorithm – Probability Learning – Sample Complexity – Finite and Infinite Hypothesis Spaces – Mistake Bound Model.

UNIT IV INSTANT BASED LEARNING **9**

K- Nearest Neighbour Learning – Locally weighted Regression – Radial Basis Functions – Case Based Learning.

UNIT V ADVANCED LEARNING **9**

Learning Sets of Rules – Sequential Covering Algorithm – Learning Rule Set – First Order Rules – Sets of First Order Rules – Induction on Inverted Deduction – Inverting Resolution – Analytical Learning – Perfect Domain Theories – Explanation Base Learning – FOCL Algorithm – Reinforcement Learning – Task – Q-Learning – Temporal Difference Learning.

TOTAL :45 PERIODS

REFERENCES

1. Tom M. Mitchell, ―Machine Learning, McGraw-Hill Education (India) Private Limited, 2013.
2. EthemAlpaydin, ―Introduction to Machine Learning (Adaptive Computation and Machine Learning), The MIT Press 2004.
3. Stephen Marsland, ―Machine Learning: An Algorithmic Perspective‖, CRC Press, 2009.

EE3506	DIGITAL CONTROL ENGINEERING	L	T	P	C
		3	0	0	3

OBJECTIVES

- To study the digital PID controllers in detail.
- To do the detailed study of signal processing in digital control.
- To do the detailed study of modeling and analysis of sampled data control system.
- To do the detailed study of design of digital control algorithms.

Subject Code:EE3506 Subject Name: Digital Control Engineering

Course Outcome – Cos		**Cognitive Skill**
CO-01	Gain knowledge about time response ,frequency response and digital PID controllers.	U,R,A
CO-02	Gain knowledge in modelling ,sampling , signal processing in digital control.	U,E
CO-03	Gain knowledge of modeling and analysis of sampled data control system.	R,U,E
CO-04	Gain knowledge of design of digital control algorithms.	U, An,.E
CO-05	Gain knowledge about the practical aspects of digital control algorithms.	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S-Synthesis

Mapping of Course Outcome with Programme Outcome

PO / **CO**	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L

CO-01	S	S	M	M	N	N	L	L	L	L	S	L
CO-02	S	S	M	M	N	N	L	L	N	L	S	L
CO-03	S	S	M	M	N	N	S	L	N	L	S	L
CO-04	S	S	M	M	N	N	S	L	L	L	S	L
CO-05	S	S	M	M	N	N	M	L	L	L	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I CONTROLLERS IN FEEDBACK SYSTEMS 9

Review of frequency and time response analysis and specifications of first and second order feedback control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9

Sampling theorem, aliasing and quantisation error, hold operation, mathematical model of sample and hold, reconstruction of analog signals, zero and first order hold, factors limiting the choice of sampling rate.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9

Difference equation description, Z-transform method of description, mapping of s-plane to z plane , pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only).

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT VPRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9

Algorithm development of PID control algorithms, finite word length effects, choice of data acquisition systems, micro controller based temperature control systems, micro controller based motor speed control systems.

TOTAL: 45 PERIODS

REFERENCES

1.M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.
2.John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
3.Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

EE3507	ADVANCED EMBEDDED SYSTEMS	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

AIM

To do an advanced study of embedded architecture, embedded processor and computing platform, networks, real time characteristics and system design techniques.

OBJECTIVES

- To study the architecture and design of embedded systems with examples.
- To do the detailed study of ARM processor architecture and design with examples.
- To study the architecture of Distributed Embedded Architecture in detail with example.
- To do the detailed study of real time characteristic approaches.
- To study the design methodologies in detail.

Subject Code: EE3507	**Subject Name: Advanced Embedded Systems**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	Understand the embedded architecture and design	U, A
CO-02	Understand the ARM processor architecture and design.	U, A
CO-03	Design the architecture of Distributed Embedded system	R, U
CO-04	Understand and study of real time characteristic approaches.	U, R,A
CO-05	Understand the design methodologies.	R, U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	L	S	M	L	L	S	N	M	N	L	N
CO-02	S	L	S	M	L	L	S	N	M	N	L	N
CO-03	S	L	S	M	L	L	S	N	M	N	L	N
CO-04	S	L	S	M	L	L	S	N	M	N	L	N
CO-05	S	L	S	M	L	L	S	N	M	N	L	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I EMBEDDED ARCHITECTURE 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioral Description, Design Example: Model Train Controller

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9

ARM processor- processor and memory organization, Data operations, Flow of Control, SHARC

processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock.

UNIT III NETWORKS 9

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link pports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS 9

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL: 45 PERIODS

REFERENCES:

1. Wayne Wolf, Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufman Publishers, 2001.
2. Jane.W.S. Liu Real-Time systems, Pearson Education Asia, 2000
3. C. M. Krishna and K. G. Shin , Real-Time Systems, ,McGraw-Hill, 1997
4. Frank Vahid and Tony Givargi Embedded System Design: A Unified Hardware/Software Introduction, s, John Wiley & Sons, 2000.

EE3572	ELECTRONIC DESIGN LABORATORY - II	**L**	**T**	**P**	**C**
		0	**0**	**2**	**1**

Aim: To design systems using PLL, CPLD, Non-adaptive and adaptive digital control system.

Objective:

- To design systems using PLL.
- To model the system using embedded micro controller.
- To design Non-adaptive and adaptive digital control system.

Subject Code: EE3572	**Subject Name: Electronic Design Laboratory – II**	
Course Outcome - COs		**Cognitive Skill**
CO-01	Analyze and design systems using PLL	An
CO-02	Analyze and design systems using CPLD	An
CO-03	Analyze and modelling the system using embedded micro controller	An

CO-04	Understand and design the non-adaptive digital control system	U
CO-05	Understand and design the adaptive digital control system	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO- J	PO-k	PO-L
CO-01	S	S	S	S	M	N	L	L	M	S	L	N
CO-02	S	S	S	S	M	N	L	L	M	S	L	N
CO-03	S	S	L	M	L	N	L	M	L	M	M	N
CO-04	S	S	L	M	L	N	L	M	L	M	M	N
CO-05	S	S	S	S	M	N	L	L	M	S	L	N

S- Strong, M- Medium, L-Low, N- Not Relevant

List of Experiments

1.System design using PIC Microcontroller.

2.Implementation of Adaptive Filters, periodogram and multistage multirate system in DSP Processor

3.Simulation of QMF using Simulation Packages

4.Modeling of Sequential Digital system using VHDL.

5.Modeling of Sequential Digital system using Verilog.

6.Design and Implementation of ALU using FPGA.

7.Simulation of NMOS and CMOS circuits using SPICE.

8.System design using 16- bit Microprocessor.

TOTAL: 45 PERIODS

OUTCOMES:

1. To design PIC microcontroller and filters.
2. Understand the VHDL language to implement in sequential circuits.
3. The performance of ALU and FPGA can be studied and analyzed.

SEMESTER-III

NO.	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	EExxx5	Elective- V	3	0	0	3
2.	OE-I	Open Elective-I	3	0	0	3
PRACTICAL						
4.	EE35P1	Project Work - Phase I	0	0	18	6
TOTAL			**6**	**0**	**18**	**12**

LIST OF PROGRAM ELECTIVES

SI. NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1.	EE35A1	Robotics	3	0	0	3
2.	EE35A2	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
3.	EE35A3	Low Power VLSI	3	0	0	3
4.	EE35A4	Internet Working and Multimedia	3	0	0	3
5.	EE35A5	DSP Integrated Circuits	3	0	0	3
6.	EE35A6	High Speed Switching Architecture	3	0	0	3
7.	EE35A7	CADD for VLSI Circuits	3	0	0	3
8.	EE35A8	Data Converters	3	0	0	3
9.	EE35A9	Advanced Digital system design	3	0	0	3
10.	EE35B1	Digital Image Processing and Applications	3	0	0	3
11.	EE35B2	VLSI Design	3	0	0	3
12.	EE35B3	High Performance Communication Networks	3	0	0	3
13.	EE35B4	Embedded Analog Interfacing	3	0	0	3

EE35A1	ROBOTICS	L	T	P	C
		3	0	0	3

Aim:

To understand the concepts in Robotics.

O**BJECTIVES**

- Robots are slowly and steadily replacing human beings in many fields. The aim of this course is to introduce the students into this area so that they could use the same when they enter the industries.
- The course has been so designed to give the students an overall view of the mechanical components
- The mathematics associated with the same.
- .Actuators and sensors necessary for the functioning of the robot.

Course Outcome - COs		Cognitive Skill
CO-01	Gain knowledge about the characteristic features of robotics	U,R,A
CO-02	Gain knowledge in automation	U,E
CO-03	Gain knowledge of sensors and sensing devices	R,U,E
CO-04	Gain knowledge of artificial intelligence	U, An,.E
CO-05	Gain knowledge integration of robot	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO-J	PO-k	PO -L
CO-01	S	S	M	M	L	S	S	S	S	L	S	L
CO-02	S	S	M	M	L	S	S	S	S	L	S	L
CO-03	S	L	M	M	L	S	M	S	S	L	S	L
CO-04	S	S	M	M	L	S	S	S	S	L	S	L
CO-05	S	S	M	M	L	S	S	S	S	L	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: INTRODUCTION TO ROBOTICS 9

Motion - Potential Function, Road maps, Cell decomposition and Sensor and sensor planning. Kinematics. Forward and Inverse Kinematics - Transformation matrix and DH transformation. Inverse Kinematics - Geometric methods and Algebraic methods. Non-Holonomic constraints.

UNIT- II: COMPUTER VISION 9

Projection - Optics, Projection on the /Image Plane and Radiometry. Image Processing - Connectivity, Images-Gray Scale and Binary Images, Blob Filling,
Thresholding, Histogram. Convolution - Digital Convolution and Filtering and Masking Techniques. Edge Detection - Mono and Stereo Vision.

UNIT-III: SENSORS AND SENSING DEVICES 9

Introduction to various types of sensor. Resistive sensors. Range sensors - Ladar (laser distance and ranging), Sonar, Radar and Infra-red. Introduction to sensing - Light sensing, Heat sensing, Touch sensing and Position sensing.

UNIT-IV: ARTIFICIAL INTELLIGENCE 9

Uniform Search strategies - Breadth first, Depth first, Depth limited, Iterative and deepening depth first search and Bidirectional search. The A* algorithm. Planning - State-Space Planning , Plan-Space Planning, Graph plan/ Sat Plan and their Comparison, Multi-agent planning 1, and Multi-agent planning 2, Probabilistic Reasoning - Bayesian Networks, Decision Trees and Bayes net inference .

UNIT-V: INTEGRATION TO ROBOT 9

Building of 4 axis or 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - AI algorithms for path finding and decision making

TOTAL: 45 PERIODS

REFERENCES:

1. Duda, Hart and Stork, *Pattern Recognition.* Wiley-Inter science, 2000.
2. Mallot, *Computational Vision: Information Processing in Perception and Visual Behavior.* Cambridge, MA: MIT Press, 2000.
3. Artificial Intelligence-A Modern Approach By Stuart Russell and Peter Norvig, Pearson Education Series in Artificial Intelligence, 2004
4. Fundamentals of Robotics, Analysis and control By Robert Schilling and Craig, Hall of India Private Limited, New Delhi, 2003.
5. Computer Vision, A modern Approach by Forsyth and Ponce, Person Education, 2003.

EE35A2	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES

To do an advanced study of electromagnetic interference and compatibility in system design.

- To study the EMI/EMC concepts and definitions in detail.
- To do the detailed study of EMI coupling.
- To study the EMI/EMC standards and measurements in detail.
- To do the detailed study of EMI control techniques.
- To study the EMC design of PCB in detail.

Course Outcome - COs		Cognitive Skill
CO-01	To know about EMI Environment	U,A
CO-02	Ability to analyze Electromagnetic interference effects in PCBs	R,A
CO-03	Ability to propose solutions for minimizing EMI in PCBs	R,U,An
CO-04	EMI Specification, Standards and Limits, EMI Measurements and Control Techniques	A
CO-05	Ability to propose solutions for minimizing EMI in PCBs	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO-J	PO-k	PO -L
CO-01	M	S	N	S	M	M	M	S	S	S	S	S
CO-02	M	S	N	M	M	M	M	S	S	S	S	S
CO-03	S	L	N	M	M	M	M	S	S	M	M	M
CO-04	S	M	L	N	L	M	M	S	S	M	M	M
CO-05	M	M	L	N	L	M	L	M	M	S	S	S

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: EMI ENVIRONMENT **9**

EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT- II: EMI COUPLING PRINCIPLES **9**

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT- III: EMI/EMC STANDARDS AND MEASUREMENTS **9**

Civilian standards - FCC,CISPR,IEC,EN,Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

UNIT-IV: EMI CONTROL TECHNIQUES **9**

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT-V: EMC DESIGN OF PCBs **9**

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

TOTAL: 45 PERIODS

REFERENCES:

1,Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", John Wiley and Sons, NewYork. 1988.

2.C.R.Paul, “Introduction to Electromagnetic Compatibility” , John Wiley and Sons, Inc, 1992

3.V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 1996.

4.Bernhard Keiser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed, 1986.

EE35A3	LOW POWER VLSI	L	T	P	C
		3	0	0	3

AIM:

To do an advanced study of ICs design, Device modeling and behavior.

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

Subject Code: EE35A3	**Subject Name: LOW POWER VLSI**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	To understand the basics of low power design	U
CO-02	Analysis of Basic low power process and devices	An
CO-03	Evaluation of device modeling and behavior	E
CO-04	To remember the Logic gates	R
CO-05	To understand the Principle Flip Flops	U

- R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	M	L	N	N	N	S	S	N	N	N	S	N
CO-02	S	N	N	N	N	L	S	N	N	N	M	N
CO-03	L	S	N	N	N	M	L	N	N	N	S	N
CO-04	S	L	N	S	N	M	S	N	N	N	M	N
CO-05	S	N	N	S	N	S	S	N	N	N	M	N

- S- Strong, M- Medium, L-Low, N- Not Relevant

UNITI POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNITII POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNITIII DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNITIV POWER ESTIMATION 9

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNITV SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:

1. Capability to recognize advanced issues in VLSI systems, specific to the deep-submicron silicon technologies.
2. Students able to understand deep submicron CMOS technology and digital CMOS design styles.
3. To design chips used for battery-powered systems and high performance circuits

TEXT BOOKS:

1.CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors) - Pearson Education Asia 1st Indian reprint, 2002

REFERENCES:

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI device devices and Circuits", John Wiley and sons, inc. 2001.

EE35A4	INTERNET WORKING AND MULTIMEDIA	L	T	P	C
		3	0	0	3

OBJECTIVES

- To introduce the characteristics of text, graphics, video and speech.
- To teach techniques for efficient transmission of multimedia signals over networks.
- To introduce different network standards and parameters for quality of service.

Course Outcome – Cos		Cognitive Skill
CO-01	Understanding about the architecture and models of multimedia communication.	U, R
CO-02	Understand and design end to end of broadband network services.	R,A
CO-03	Build the multicast routing and guaranteed service models.	A

CO-04	Provide the end to end solutions for multimedia services on demand.	An
CO-05	To built the various Multimedia Communication tasks.	A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	M	S	L	S	M	L	M	N	L	L	N
CO-02	L	S	M	L	M	S	M	M	N	N	L	N
CO-03	M	L	L	N	S	M	S	S	N	L	M	N
CO-04	L	S	S	N	L	L	S	S	N	M	S	N
CO-05	S	M	N	N	M	M	M	M	N	M	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: MULTIMEDIA NETWORKING 9

Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT- II : BROAD BAND NETWORK TECHNOLOGY 9

Broadband services, ATM and IP , IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT-III: MULTICAST AND TRANSPORT PROTOCOL 9

Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT- IV: MEDIA - ON – DEMAND 9

Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT –V: APPLICATIONS 9

MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

TOTAL: 45 PERIODS

REFERENCES:

1.Jon Crowcroft, Mark Handley, Ian Wakeman. Internetworking Multimedia, Harcourt Asia Pvt.Ltd.Singapore, 1998.
2.B.O. Szuprowicz, Multimedia Networking, McGraw Hill, NewYork. 1995.
3.Tay Vaughan, Multimedia making it to work, 4ed,Tata McGrawHill, NewDelhi, 2000.

EE35A5	DSP INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

Aim:

To gain knowledge in DSP integrated circuits.

OBJECTIVES

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite word length effects.
- To know about the basic DSP processor architectures and the synthesis of the processing elements.
- To gather an idea about the VLSI circuit layout design styles.

Course Outcome – Cos		Cognitive Skill
CO-01	Gain knowledge in DSP and DSP algorithms	U,R,A
CO-02	Gain knowledge in digital filters and finite word length effects	U,E
CO-03	Gain knowledge in DSP architecture	R,U
CO-04	Gain knowledge in synthesis of DSP architecture	U, S.E
CO-05	Gain knowledge integrated circuit design	R,A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO-J	PO-k	PO -L
CO-01	S	S	M	M	N	N	L	L	L	L	S	L
CO-02	S	S	M	M	N	N	L	M	N	L	S	L
CO-03	S	S	M	M	N	N	S	L	N	L	S	L
CO-04	S	S	M	M	N	N	S	L	L	L	S	L
CO-05	S	S	M	M	N	N	M	L	L	L	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I : INTRODUCTION TO DSP INTEGRATED CIRCUITS 9

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms, Standard digital signal procesors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT- II: DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length

effects –Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT-III: DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture.TMS320C54x and TMS320C6x architecture, Motorola DSP56002 architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures.

UNIT- IV: SYNTHESIS OF DSP ARCHITECTURES AND ARITHMETIC UNIT 9

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Arithmetic Unit : Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator.

UNIT V CASE STUDY-INTEGRATED CIRCUIT DESIGN 9

Layout of VLSI circuits, Layout Styles, Case Study: FFT processor, DCT processor and Interpolator.

TOTAL: 45 PERIODS

REFERENCES:

1. Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education,2002.
3. B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002.
4. Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Tata McGraw-Hill, 2002.
5. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

EE35A6	HIGH SPEED SWITCHING ARCHITECTURE	L	T	P	C
		3	0	0	3

OBJECTIVES

- To highlight the features of different technologies involved in High speed Networking and their performance
- Students will get an introduction about various high speed networks.
- Students will be provided with an up-to-date survey of developments in High Speed Networks..
- Enable the students to know techniques involved in LAN switching and ATM switching.
- Students will get an introduction about various Queuing techniques involved in high speed networks

Course Outcome - COs		Cognitive Skill
CO-01	To understand the basic concepts of High-Speed Networks.	U
CO-02	Apply the various switching techniques in ATM and LAN networks	A
CO-03	Analyze various queuing techniques in ATM switches.	An

CO-04	Design and develop the IP switching networks	An
CO-05	Understand various switching networks	U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	L	L	S	L	S	L	M	S	S	N	S	M
CO-02	S	L	M	S	S	M	S	S	M	N	M	S
CO-03	M	M	M	S	L	M	L	S	S	N	M	L
CO-04	M	M	M	S	L	M	L	S	S	N	M	L
CO-05	L	L	S	L	S	L	M	S	S	N	S	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: HIGH SPEED NETWORK 9

Introduction- LAN, WAN, Network evolution through ISDN to B-ISDN, Transfer mode and control of B-ISDN, SDH multiplexing structure, ATM standard, ATM adaptation layers.

UNIT- II: LAN SWITCHING TECHNOLOGY 9

Switching Concepts, switch forwarding techniques, switch path control, LAN Switching, cut through forwarding, store and forward, virtual LANs

UNIT- III: ATM SWITCHING ARCHITECTURE 9

Switch model, Blocking networks - basic - and- enhanced banyan networks, sorting networks - merge sorting, rearrangeable networks - full-and- partial connection networks, non blocking networks - Recursive network construction, comparison of non-blocking network, Switching with deflection routing - shuffle switch, tandem banyan

UNIT- IV: QUEUES IN ATM SWITCHES 9

Internal Queueing -Input, output and shared queueing, multiple queueing networks – combined Input, output and shared queueing - performance analysis of Queued switches.

UNIT-V: IP SWITCHING 9

Addressing model, IP Switching types - flow driven and topology driven solutions, IP Over ATM address and next hop resolution, multicasting, Ipv6 over ATM.

TOTAL: 45 PERIODS

REFERENCES:

1.Achille Pattavina, Switching Theory: Architectures and performance in Broadband ATM networks "John Wiley & Sons Ltd, New York. 1998

2.Christopher Y Metz, Switching protocols & Architectures, McGraw - Hill Professional Publishing, NewYork.1998.

3.Rainer Handel, Manfred N Huber, Stefan Schroder, ATM Networks - Concepts Protocols, Applications III Edition, Addison Wesley, New York. 1999.

4.John A.Chiong: Internetworking ATM for the internet and enterprise networks. McGraw Hill, New York, 1998.

EE35A7	CADD FOR VLSI CIRCUITS	L	T	P	C
		3	0	0	3

Aim:

To gain knowledge in CADD for VLSI circuits.

OBJECTIVES

- The design of all VLSI circuits is carried out by making extensive use Computer Aided Design (CAD) VLSI design tool. Due to continuous scaling of semiconductor technology, most of the VLSI designs employ millions of transistors and circuits of this size can only be carried out with the aid of CAD VLSI design tools.
- The VLSI design professional needs to have a good understanding of the operation of these CAD VLSI design tools as these are developed primarily for and by the VLSI design professionals.

Course Outcome – Cos		**Cognitive Skill**
CO-01	Design advanced electronics systems	U
CO-02	Evaluate and analyze the systems in VLSI design environments	E
CO-03	Apply advanced technical knowledge in multiple contexts	A
CO-04	systematic study on significant research topic within the field of VLSI	An
CO-05	Conduct an organized and systematic study on significant research topic within the allied field.	An

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO **CO**	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	L	L	S	L	S	L	M	S	S	N	S	M
CO-02	S	M	M	M	L	S	L	M	S	L	M	M
CO-03	S	L	M	S	S	M	S	S	M	N	M	S
CO-04	M	M	M	S	L	M	L	S	S	N	M	L
CO-05	L	L	S	L	S	L	M	S	S	N	S	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT- II: DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning.

UNIT- III: FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT- IV: SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT- V: MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL: 45 PERIODS

REFERENCES:

1.S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2.N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

EE35A8	DATA CONVERTERS	L	T	P	C
		3	0	0	3

Aim:

To understand data converters

OBJECTIVES

- Analog to Digital (AD) and Digital to Analog (DA) converters constitute a very important building block in all electronics systems. It is these blocks which provide the crucial interface between the primarily analog real world signals and the predominantly digital electronic systems.
- These are critical blocks which are utilized in all major industrial sectors including computers, wireless communication, audio and video systems, biomedical systems, aerospace and automotive systems and so on. There are a few established circuit architectures and principles for design of AD and DA converters.

Course Outcome – Cos		Cognitive Skill
CO-01	Evolution of converters	R
CO-02	Compute Switched-capacitor amplifiers	A
CO-03	performance metrics of ADCs and DACs	A
CO-04	Pipelined Architecture	A
CO-05	Sigma delta modulator characteristics.	S

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	S	S	S	S	S	S	L	L	L	L	L
CO-02	S	M	M	S	M	M	M	M	N	N	N	N

CO-03	S	S	S	M	M	M	M	L	N	N	N	N
CO-04	S	M	M	M	M	S	S	L	N	N	N	N
CO-05	S	S	S	S	S	M	M	L	N	N	N	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I : INTRODUCTION AND CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS 9

Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

UNIT- II: SWITCH CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques.

UNIT- III: NYQUIST RATE D/A CONVERTERS 9

Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs.

UNIT- IV: PIPELINE AND OTHER ADCs 9

Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT –V: SIGMA DELTA CONVERTERS 9

STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Op amp nonlinearities.

TOTAL: 45 PERIODS

REFERENCES:

1.Behzad Razavi, “Principles of data conversion system design”, IEEE press, 1995.

2.M. Pelgrom, Analog-to-Digital Conversion, Springer, 2010.

3.Rudy van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters” Kluwer Acedamic Publishers, Boston, 2003.

4.R. Schreier, G. Temes, Understanding Delta-Sigma DataConverters, Wiley-IEEE Press, 2004

5.J. G. Proakis, D. G. Manolakis, Digital Signal Processing,Prentice Hall, 1995

6.VLSI Data Conversion Circuits EE658 recorded lectures available at http://www.ee.iitm.ac.in/~nagendra/videolecture

EE35A9	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
		3	0	0	3

AIM

To do an advanced study of sequential circuit design, asynchronous sequential circuit design, fault diagnosis and testability algorithms, synchronous design using programmable devices and system design using VHDL.

OBJECTIVES:

- To introduce methods to analyse and design synchronous sequential circuits
- *To introduce methods to analyse and design asynchronous sequential circuits and to analyse hazards
- *To introduce the fault testing procedure for combinational circuits and PLA circuits
- *To introduce the architectures of programmable devices
- *To introduce design and implementation of digital circuits using programming tools

Subject Code:EE35A9	**Subject Name: ADVANCED DIGITAL SYSTEM DESIGN**	
Course Outcome – Cos		**Cognitive Skill**
CO-01	To understand about sequential circuit	R
CO-02	Apply ASC to find races	A
CO-03	To understand about different faults	U
CO-04	Analyze the programmable devices	an
CO-05	Design and synthesis using VHDL	s

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / **CO**	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO - I	PO-J	PO-k	PO -L
CO-01	S	L	M	M	M	S	S	M	N	N	S	N
CO-02	S	N	M	M	M	L	S	M	N	N	M	N
CO-03	S	S	M	M	M	M	L	M	N	N	S	N
CO-04	S	L	M	S	L	M	S	M	N	N	M	N
CO-05	S	N	M	S	L	S	S	M	N	N	M	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuit's design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method - D algorithm – Kohavi algorithm – Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Designing ROM with PLA – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

TOTAL: 45 PERIODS

OUTCOMES:

1. Analyse and design synchronous sequential circuits
2. Analyse hazards and design asynchronous sequential circuits
3.Knowledge on the testing procedure for combinational circuit and PLA
4.Able to design PLD and ROM
5.Design and use programming tools for implementing digital circuits of industry

REFERENCES:

1. Charles H.Roth Jr, “Fundamentals of Logic Design”, Thomson Learning, 2004.
2. M.D.Ciletti , “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, Prentice Hall, 1999.
3. M.G.Arnold, “Verilog Digital – Computer Design”, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas,“Logic Design Theory”, Prentice Hall of India,2001.
5. Parag K. Lala, “Fault Tolerant and Fault Testable Hardware Design”, B S Publications,2002.
6. Parag K.Lala, “Digital system Design using PLD”, B S Publications, 2003.
7. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003.

EE35B1	DIGITAL IMAGE PROCESSING AND APPLICATIONS	L	T	P	C
		3	0	0	3

Aim:

To study concepts in DIGITAL IMAGE PROCESSING AND APPLICATIONS

OBJECTIVES

- To introduce the student to various image processing techniques such as enhancements, segmentation, compression etc.
- To study the image fundamentals and mathematical transforms necessary for image processing.
- To study the image enhancement techniques
- To study image restoration procedures.
- To study the image compression procedures.
- To study the image segmentation and representation techniques.

Course Outcome – Cos	Cognitive Skill

CO-01	Review the fundamental concepts of a digital image processing system.	R
CO-02	Analyze images in the frequency domain using various transforms	An
CO-03	Evaluate the techniques for image enhancement and image restoration	E
CO-04	Categorize various compression techniques	U
CO-05	Interpret image segmentation and representation techniques.	R

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	M	s	M	M	M	S	S	L	L	S	M
CO-02	M	M	S	M	M	M	S	S	L	L	S	M
CO-03	M	S	M	S	M	M	M	M	M	M	M	M
CO-04	M	S	M	S	M	M	M	S	M	S	M	M
CO-05	M	M	M	M	M	M	M	S	L	L	L	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I : DIGITAL IMAGE FUNDAMENTALS AND TRANSFORMS 9

Elements of digital image processing systems, Elements of visual perception, psycho visual model, brightness, contrast, hue, saturation, mach band effect, Image Transforms - Discrete Cosine Transform, Walsh Transform, Hadamard Transform, Slant Transform, Haar Transform Discrete Wavelet Transform.

UNIT –II: IMAGE ENHANCEMENT AND RESTORATION 9

Histogram modification and specification techniques, Noise distributions, Spatial averaging, Homomorphic filtering, Pseudo Color image processing, Full color image processing. Image Restoration – degradation model, Unconstrained and Constrained restoration, Wiener filtering, Geometric transformations – spatial transformations, Gray-Level interpolation.

UNIT- III: IMAGE SEGMENTATION, REPRESENTATION AND DESCRIPTION9

Point, Line and Edge detection – Edge linking via Hough transform – Thresholding – Region based segmentation, Region growing, Region splitting and Merging – Image representation schemes – Boundary descriptors – Regional descriptors – Relational descriptors.

UNIT –IV: IMAGE COMPRESSION 9

Need for data compression, Huffman, Shannon Fano Coding, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding. Transform Coding – DCT, JPEG, MPEG Standards.

UNIT –V: APPLICATIONS 9

Imaging Applications: Patterns and Pattern classes, Optical character Recognition- Rule based Character Recognition- Face and Facial feature Extraction - Video motion Analysis- Image Fusion- Watermarking – spatial & frequency domain

TOTAL: 45 PERIODS

REFERENCES:

1.Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.
2.Anil K. Jain, 'Fundamentals of Digital Image Processing', Prentice Hall of India, 2002.
3.David Salomon : Data Compression – The Complete Reference, Springer Verlag New York Inc., 2nd Edition, 2001
4.Rafael C. Gonzalez, Richard E.Woods, Steven Eddins, ' Digital Image Processing using MATLAB', Pearson Education, Inc., 2004.
5.William K.Pratt, ' Digital Image Processing', John Wiley, NewYork, 2002.
6.MilmanSonka, Vaclav Hlavac, Roger Boyle, 'Image Processing, Analysis, and Machine Vision', Brooks/Cole, Vikas Publishing House, II ed., 1999.
7.Sid Ahmed, M.A., 'Image Processing Theory, Algorithms and Architectures', McGrawHill, 1995.

EE35B2	VLSI DESIGN	L	T	P	C
		3	0	0	3

AIM

To do an advanced study of VLSI system component design techniques.

OBJECTIVES

- Analyze the characteristics of MOS transistor.
- Understand various CMOS fabrication techniques.
- Identify latch up problems in CMOS circuits.
- Illustrate the concepts of CMOS inverters and their sizing methods.
- Estimate Power and delay in CMOS circuits.

Subject Code: EE35B2	**Subject Name: VLSI DESIGN**	
	Course Outcome – Cos	**Cognitive Skill**
CO-01	Understand the Conventional design procedure MOS transistor theory and process technology	U, A
CO-02	Understand the basics of inverters and logic gates.	U, A
CO-03	Design the circuit and estimate the performance of the circuit	R, U
CO-04	Understand and remember system components using VLSI techniques.	U, R,A
CO-05	Design the digital components using verilog hardware description language	R, U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	M	S	L	M	L	L	S	N	M	N	L	L
CO-02	M	S	L	M	L	L	S	N	M	N	L	L
CO-03	M	S	L	M	L	L	S	N	M	N	L	L
CO-04	M	S	L	M	L	L	S	N	M	N	L	L

CO-05	M	S	L	M	L	L	S	N	M	N	l	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I **9**

MOS TRANSISTOR THEORY

NMOS and PMOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model..

UNIT II **9**

CMOS TECHNOLOGY AND DESIGN RULE

CMOS fabrication and Layout, CMOS technologies, P -Well process, N -Well process, twin -tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology – related CAD issues, Fabrication and packaging.

UNIT III **9**

INVERTERS AND LOGIC GATES

NMOS and CMOS Inverters, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design..

UNIT IV **9**

CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION.

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT V **9**

VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN

Multiplexers, Decoders , comparators, priority encoders , shift registers, Arithmetic circuits-Ripple carry adders, Carry look ahead adders, High-speed adders,Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

TOTAL: 45 PERIODS

OUTCOMES:

After successful completion of the course student will be able to:

1. Demonstrate a clear understanding of CMOS (Permanently Affiliated to University of Mumbai)
2. Design MOSFET based logic circuit
3. Draw layout of a given logic circuit
4. Realize logic circuits with different design styles
5. Demonstrate an understanding of working principle of operation of different types of memories
6. Demonstrate an understanding of working principles of clocking, power reduction and distribution

REFERENCES:

1.Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2.John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., 2002.
3.Eugene D. Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.
4.Pucknell, “Basic VLSI Design”, Prentice Hall of India Publication, 1995.
5.Wayne Wolf “Modern VLSI Design System on chip. Pearson Education.2002.

EE35B3	HIGH PERFORMANCE COMMUNICATION NETWORKS	L	T	P	C
		3	0	0	3

Aim:

To study high performance communication networks

OBJECTIVES:

- To ensure a comprehensive understanding of high speed computer network architectures
- To study mathematical models related to network performance analysis.
- To focus on current and emerging networking technologies.

UNIT I PACKET SWITCHED NETWORKS 9

OSI and IP models, Ethernet (IEEE 802.3), Token ring (IEEE 802.5), Wireless LAN (IEEE 802.11) DQDB, ISDN and Broadband ISDN architecture and Protocols.

UNIT II ATM AND FRAME RELAY 9

ATM: Main features-addressing, signaling and routing, ATM header structure-adaptation layer, management and control, ATM switching and transmission.

Frame Relay: Protocols and services, Congestion control, Internetworking with ATM, Internet and ATM, Frame relay via ATM.

UNIT III ADVANCED NETWORK ARCHITECTURE 9

IP forwarding architectures overlay model, Multi Protocol Label Switching (MPLS), integrated services in the Internet, VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.

UNIT IVBLUE TOOTH TECHNOLOGY 9

The Blue tooth module-Protocol stack Part I: Antennas, Radio interface, Base band, The Link controller, Audio, The Link Manager, The Host controller interface; The Blue tooth module-Protocol stack Part I: Logical link control and adaptation protocol.

UNIT V MULTIMEDIA NETWORKING APPLICATIONS 9

Streaming stored Audio and Video, Best effort service, protocols for real time interactive applications, Beyond best effort, scheduling and policing mechanism, integrated services, Resource Reservation Protocol (RSVP), Differentiated services

TOTAL: 45 PERIODS

OUTCOMES:

1.To design High performance computer networks.

2.To design and implement CAC protocols in multimedia networks.

3.Design and implement network protocols in HPCN.

3.Analyse performance of network related issues using mathematical models.

4.Compare the various methods of providing connection-oriented services over an advanced network with reference to MPLS, VPN.

REFERENCES:

1. Aunurag Kumar, D. Manjunath, Joy Kuri, “Communication Networking”, Morgan Kaufmann Publishers, 2011.

2. J.F. Kurose & K.W. Ross, “Computer Networking- A Top Down Approach Featuring the Internet”, Pearson, 2nd Edition, 2003.

3. Nader F.Mir, “Computer and Communication Networks”, Pearson Education, 2009.

4. Walrand .J. Varatya, “High Performance Communication Network”, Morgan Kaufmann – Harcourt Asia Pvt. Ltd., 2nd Edition, 2000.

5. HersentGurle& petit, “IP Telephony, Packet Pored Multimedia Communication Systems”, Pearson Education 2003.
6. Fred Halsall and Lingana Gouda Kulkarni, “Computer Networking and the Internet”, Fifth Edition, Pearson Education, 2012.
7. Larry L.Peterson & Bruce S.David, “Computer Networks: A System Approach”- Morgan Kaufmann Publisher, 1996.

EE35B4	EMBEDDED ANALOG INTERFACING	L	T	P	C
		3	0	0	3

Aim:

To study embedded analog interfacing

OBJECTIVES

To do an advanced study of measurement system design, analog to digital converters, sensors and peripherals, output control methods and micro controller interfacing

- To do a detailed study of measurement system design.
- To study the analog to digital converters in detail.
- To study the sensors and peripherals in detail.
- To do the detailed study of output control methods.
- To study in detail about the micro controller interfacing.

Course Outcome – Cos		Cognitive Skill
CO-01	Understand the characteristics of measurement	U, A
CO-02	Understand the concept of analog to digital converters.	U, A
CO-03	Understand the concept of sensors and peripherals	R, U
CO-04	Understand and various control methods.	U, R,A
CO-05	Understand microcontroller interfacing.	R, U

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO- C	PO-D	PO- E	PO- F	PO-G	PO-H	PO - I	PO- J	PO- k	PO -L
CO-01	S	L	M	M	S	L	S	N	M	N	L	N
CO-02	S	L	M	M	S	L	S	N	M	N	L	N
CO-03	S	L	M	M	S	L	S	N	M	N	L	N

CO-04	S	L	M	M	S	L	S	N	M	N	L	N
CO-05	S	L	M	M	S	L	S	N	M	N	l	N

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT –I: **MEASUREMENT SYSTEM DESIGN** **9**

Characteristics of Instrumentation – Measurement accuracy – Measurement standards - Dynamic Range – Calibration – Bandwidth – Digital interfacing advantages

UNIT- II: ANALOG-TO-DIGITAL CONVERTERS **9**

Types of ADCs - ADC Comparison - Sample and Hold - ADC Types - Flash ADC - Successive Approximation ADC - Dual-Slope (Integrating) ADC - Sigma-Delta ADC - Microprocessor Interfacing - Clocked Interfaces - Serial Interfaces – Integrated ADC Embedded Controllers

UNIT- III: SENSORS & PERIPHERALS **9**

Temperature Sensors - Optical Sensors – CCDs - Magnetic Sensors - Motion/Acceleration Sensors - Strain Gauges - Solenoids – Heaters – Coolers – LEDs – DACs - Digital Potentiometers - Analog Switches - Stepper Motors - DC Motors

UNIT- IV*:* **OUTPUT CONTROL METHODS** **9**

Measuring Period versus Frequency - Voltage-to-Frequency Converters - Open-Loop Control - Negative Feedback and Control - Microprocessor-Based Systems- On-Off Control - Proportional Control - Proportional, Integral, Derivative Control - Motor Control - Predictive Control - Measuring and Analyzing Control Loops

UNIT- V : **MICROCONTROLLER INTERFACING** **9**

Standard Interfaces - IEEE 1451.2 - 4–20 ma Current Loop – Fieldbus - Microcontroller Supply and Reference - Resistor Networks - Multiple Input Control -AC Control - Voltage Monitors and Supervisory Circuits - Driving Bipolar Transistors/ MOSFET- Reading Negative Voltages – PWM based control

TOTAL: 45 PERIODS

REFERENCES:

1.Analog Interfacing to Embedded Microprocessor Systems by Stuart R. Ball.
2.The measurement, Instrumentation, & sensors Handbook by John G. Webster.
3.Microcontroller-Based Temperature Monitoring and Control by by Dogan Ibrahim.

LIST OF OPEN ELECTIVES

SI. NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1.	EC35B1	Fundamental of Soft Computing Techniques	3	0	0	3
2.	GE35A1	Business Analytics	3	0	0	3
3.	GE35A2	Industrial Safety	3	0	0	3
4.	GE35A3	Operations Research	3	0	0	3
5.	GE35A4	Cost Management of Engineering Projects	3	0	0	3

6.	GE35A5	Composite Materials	3	0	0	3
7.	GE35A6	Waste to Energy	3	0	0	3

OPEN ELECTIVES

EC35B1	FUNDAMENTAL OF SOFT COMPUTING TECHNIQUES	L	T	P	C
		3	0	0	3

Aim:

To understand the fundamental of soft computing techniques.

OBJECTIVES

- To introduce the techniques of soft computing and adaptive neuro-fuzzy inferencing systems which differ from conventional AI and computing in terms of its tolerance to imprecision and uncertainty.
- To introduce the ideas of fuzzy sets, fuzzy logic and use of heuristics based on human experience
- To become familiar with neural networks that can learn from available examples and generalize to form appropriate rules for inferencing systems
- To provide the mathematical background for carrying out the optimization associated with neural network learning
- To familiarize with genetic algorithms and other random search procedures useful while seeking global optimum in self-learning situations

Course Outcome – Cos		Cognitive Skill
CO-01	To understand the concepts of ANN, different features of fuzzy logic and their modeling, control aspects and different hybrid control schemes.	U
CO-02	To understand the basics of artificial neural network.	U
CO-03	To get knowledge on modeling and control of artificial neural network.	R
CO-04	To get knowledge on modeling and control of fuzzy control schemes.	U, R
CO-05	To acquire knowledge on hybrid control schemes.	A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO- I	PO-J	PO-k	PO-L
CO-01	M	M	S	M	M	S	S	M	S	N	M	M
CO-02	M	M	S	M	M	S	M	M	S	N	M	M
CO-03	M	M	S	M	M	S	M	M	S	N	S	L
CO-04	M	M	S	M	M	S	M	M	S	N	M	L

CO-05	M	M	S	M	M	S	M	M	S	N	M	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT- I: ARTIFICIAL NEURAL NETWORKS 9

Basic concepts-single layer perceptron-Multi layer perceptron-Adaline-Madaline-Learning rules-Supervised learning-Back propagation networks-Training algorithm, Practical difficulties, Advanced algorithms-Adaptive network- Radial basis network-modular network-Applications

UNIT- II: UNSUPERVISED NETWORKS 9

Introduction- unsupervised learning -Competitive learning networks-Kohonen self organising networks-Learning vector quantisation - Hebbian learning - Hopfield network-Content addressable nature, Binary Hopfield network, Continuous Hopfield network Travelling Salesperson problem - Adaptive resonance theory –Bidirectional Associative Memory-Principle component Analysis

UNIT- III: FUZZY SYSTEMS 9

Fuzzy sets-Fuzzy rules: Extension principle, Fuzzy relation- fuzzy reasoning – fuzzy inference systems: Mamdani model, Sugeno model. Tsukamoto model -Fuzzy decision making- Multi objective Decision Making,-Fuzzy classification-Fuzzy control methods -Application

UNIT- IV: NEURO-FUZZY MODELLING 9

Adaptive Neuro Fuzzy based inference systems – classification and regression trees: decision tress, Cart algorithm – Data clustering algorithms: K means clustering, Fuzzy C means clustering, Mountain clustering, Subtractive clustering – rule base structure identification – Neuro fuzzy control: Feedback Control Systems, Expert Control, Inverse Learning, Specialized Learning, Back propagation through Real –Time Recurrent Learning.

UNIT –V: GENETIC ALGORITHM 9

Fundamentals of genetic algorithm-Mathematical foundations-Genetic modeling-Survival of the fittest-crossover-Inversion and Deletion-mutation-reproduction-Generational cycle-rank method-rank space method- Other derivative free optimization-simulated annealing, Random search, Downhill simplex search-Application

TOTAL: 45 HOURS

REFERENCES

1.Jang J.S.R.,Sun C.T and Mizutani E – "Neuro Fuzzy and Soft computing", Pearson education (Singapore) 2004

2.David E.Goldberg : "Genetic Algorithms in Search, Optimization, and Machine Learning", Pearson Education, Asia, 1996

3.LaureneFauseett:"Fundamentals of Neural Networks", Prentice Hall India, New Delhi,1994.

4.Timothy J.Ross:"Fuzzy Logic Engineering Applications", McGraw Hill, NewYork, 1997.

5.S.Rajasekaran and G.A.VijayalakshmiPai "Neural networks,Fuzzylogics,and Genetic algorithms", Prentice Hall of India, 2003

6.George J.Klir and Bo Yuan,"Fuzzy Sets and Fuzzy Logic",Prentice Hall Inc., New Jersey, 1995

GE35A1	**BUSINESS ANALYTICS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

AIM:

To understand the basic concepts of Business Analytics and other operational techniques.

OBJECTIVES:

- To make students understandable about the Regression Analysis, Business analytics, forecasting and decision analysis.

Subject Code: GE35A1	**Subject Name:BUSINESS ANALYTICS**	
Course Outcome - COs		**Cognitive Skill**
CO-01	Ability to understand the concepts of Business Analytics.	U,R
CO-02	Can understand the factors of Trendiness and Regression analysis.	U,R
CO-03	Students can understand about organization structures of business analytics.	U,R
CO-04	One can understand the concepts of Forecasting Techniques.	U,R
CO-5	Can understand the Decision analysis.	U,R

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	S	M	M	M	S	S	M	S	S	S	M
CO-02	S	S	M	M	M	S	S	M	S	S	S	M
CO-03	S	S	M	M	M	S	S	M	S	S	S	M
CO-04	S	S	M	M	M	S	S	M	S	S	S	M
CO-05	S	S	M	M	M	S	S	M	S	S	S	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I- BUSINESS ANALYTICS: 9

Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics.

Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modeling, sampling and estimation methods overview.

UNIT II- TRENDINESS AND REGRESSION ANALYSIS: 9

Modeling Relationships and Trends in Data, simple Linear Regression.

Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT III- ORGANIZATION STRUCTURES OF BUSINESS ANALYTICS: 9

Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes.

Descriptive Analytics, predictive analytics, predicative Modeling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modeling, nonlinear Optimization.

UNIT IV- FORECASTING TECHNIQUES: 9

Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT V- DECISION ANALYSIS: 9

Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making. Recent Trends in : Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

TOTAL: 45 HOURS

REFERENCES:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G.Schniederjans, Christopher M. Starkey, Pearson FT Press.2014
2. Business Analytics by James Evans, persons Education.3rd edition 2018

GE35A	INDUSTRIAL SAFETY	L	T	P	C
		3	0	0	3

AIM:

To understand the basic Industrial Safety and Fault diagnosis.

OBJECTIVES:

- To make students understandable about the Industrial safety, Maintenance and fault tracing.

Subject Code: GE35A2	**Subject Name:**INDUSTRIAL SAFETY	
Course Outcome - COs		**Cognitive Skill**
CO-01	Ability to understand the concepts of Industrial Safety.	R,U
CO-02	Can understand the fundamentals of Maintenance Engineering.	R,U,A
CO-03	Students can understand the ways to prevent from wear and corrosion.	R,U,A
CO-04	One can understand the concepts of fault tracing.	R,U,A
CO-05	Can understand the functions of periodic and preventive maintenance.	A

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	M	M	L	L	S	M	S	M	S	S	S
CO-02	M	S	M	M	L	S	M	M	S	S	S	S
CO-03	M	M	L	S	L	S	S	M	M	M	S	S
CO-04	M	S	L	M	L	S	M	S	S	M	S	L
CO-05	M	S	L	M	L	S	S	S	M	S	S	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT IINDUSTRIAL SAFETY: 9

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash

rooms, drinking water layouts, light, leanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT IIFUNDAMENTALS OF MAINTENANCE ENGINEERING: 9

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT IIIWEAR AND CORROSION AND THEIR PREVENTION: 9

Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IVFAULT TRACING: 9

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Anyone machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT VPERIODIC AND PREVENTIVE MAINTENANCE: 9

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance.

TOTAL: 45 HOURS

REFERENCES

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

GE35A3	OPERATIONS RESEARCH	L	T	P	C
		3	0	0	3

AIM:

To understand the concepts behind Operations Research.

OBJECTIVES:

- To make students understandable about the optimization techniques

Subject Code: GE35A3 **Subject Name:** OPERATIONS RESEARCH		
Course Outcome - COs		**Cognitive Skill**
CO-01	Ability to understand the concepts of Optimization Techniques.	U, An
CO-02	Can understand the fundamentals of LPP formulation.	U, An

CO-03	Students can understand the Non-Linear Programming.	U, An
CO-04	One can understand the concepts Scheduling and Sequencing.	U, An
CO-05	Can understand the functions of Competitive models.	U, An

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	S	M	L	L	M	S	M	S	S	S	L
CO-02	S	S	S	M	L	M	S	M	S	S	S	L
CO-03	S	S	S	L	L	M	S	M	S	S	S	L
CO-04	S	S	S	L	L	M	S	M	S	S	S	L
CO-05	S	S	S	L	L	M	S	M	S	S	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT IOPTIMIZATION TECHNIQUES: 9

Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT II LPP FORMULATION: 9

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

UNIT III NONLINEAR PROGRAMMING: 9

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

UNIT IV SCHEDULING AND SEQUENCING: 9

Single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT V COMPETITIVE MODELS: 9

Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation.

TOTAL: 45 HOURS

REFERENCES

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

GE35A4	COST MANAGEMENT OF ENGINEERING PROJECTS	L	T	P	C
		3	0	0	3

AIM:

To understand the concepts of Cost management of Engineering Projects.

OBJECTIVES:

- To make students understandable about the cost concepts in decision making and profit planning.

Subject Code: GE35A4 **Subject Name:** COST MANAGEMENT OF ENGINEERING PROJECTS

Course Outcome - COs		Cognitive Skill
CO-01	Ability to understand the strategic cost management.	U
CO-02	Can understand the fundamentals of cost concepts in decision making.	U,A
CO-03	Students can understand the process involved in project execution.	A
CO-04	One can understand the concepts of cost behavior and profit planning.	A
CO-05	Can understand the functions of quantitative techniques.	A,An

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	s	M	L	L	M	M	M	L	S	S	L
CO-02	S	S	M	L	L	M	S	S	L	S	S	L
CO-03	S	s	S	L	L	M	M	M	L	S	S	L
CO-04	S	S	S	L	L	M	M	M	L	S	S	L
CO-05	S	S	M	L	L	M	S	S	L	S	S	L

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT ISTRATEGIC COST MANAGEMENT: **9**

Introduction and Overview of the Strategic Cost Management Process.

UNIT II COST CONCEPTS IN DECISION MAKING: **9**

Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT III PROJECT: **9**

Meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts.Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

UNIT IVCOST BEHAVIOR AND PROFIT PLANNING: 9

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems .Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT V QUANTITATIVE TECHNIQUES: 9

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

TOTAL: 45 HOURS

REFERENCES

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler Publisher
5.N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

GE35A5	COMPOSITE MATERIALS	L	T	P	C
		3	0	0	3

AIM:

To understand the characterization and properties of composite materials.

OBJECTIVES:

- To make students understandable about the material characteristics, processing and classifications of composite materials.

Subject Code: GE35A5	**Subject Name:** COMPOSITE MATERIALS	
Course Outcome - COs		**Cognitive Skill**
CO-01	Ability to understand the functional requirements of composite materials.	U,A
CO-02	Can understand the properties and applications of reinforcements.	U,A
CO-03	Students can understand the process involved in metal matrix composite fabrication.	U,A
CO-04	One can understand the concepts of polymer matrix composites fabrication.	U,A,AN
CO-05	Can understand the physical characteristics of composite materials.	R,U,AN

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO-J	PO-k	PO-L
CO-01	S	M	M	L	L	S	M	S	M	S	S	S
CO-02	S	S	M	M	L	S	M	M	S	S	S	S
CO-03	S	M	S	S	L	S	S	M	M	M	S	S
CO-04	S	S	S	M	L	S	M	S	S	M	S	L
CO-05	S	S	M	M	L	S	S	S	M	S	S	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT IINTRODUCTION: **9**

Definition – Classification and characteristics of Composite materials. Advantages and application of composites.Functional requirements of reinforcement and matrix.Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT IIREINFORCEMENTS: **9**

Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers.Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT IIIMANUFACTURING OF METAL MATRIX COMPOSITES: **9**

Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing.Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNITIVMANUFACTURING OF POLYMER MATRIX COMPOSITES: **9**

Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression molding – Reaction injection moulding. Properties and applications.

UNIT V STRENGTH: **9**

Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygro thermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TOTAL: 45 HOURS

TEXT BOOKS

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

REFERENCES

1. Hand Book of Composite Materials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L. Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

GE35A6	WASTE TO ENERGY	L	T	P	C
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AIM:

To understand the basic properties of Bio Materials and its process

OBJECTIVES:

To make students understandable about the gasification process, bio materials and its design considerations.

Subject Code:GE35A6	**Subject Name**:WASTE TO ENERGY	
Course Outcome - COs		**Cognitive Skill**
CO-01	Ability to understand the process of obtaining Energy from waste substances.	U
CO-02	Can understand manufacturing of pyrolytic oils and gases, yields and applications.	A
CO-03	Students can understand kinetic consideration in gasifier operation.	U
CO-04	One can understand the Design, construction and operation of Bio Mass chamber.	E
CO-05	Can understand the basic Properties of biogas	R

R- Remember, U-Understand, A-Apply, An-Analyze, E-Evaluate, S- Synthesis

Mapping of Course Outcome with Programme Outcome

PO / CO	PO-A	PO-B	PO-C	PO-D	PO-E	PO-F	PO-G	PO-H	PO-I	PO- J	PO-k	PO-L
CO-01	S	M	M	M	M	M	M	M	M	M	L	M
CO-02	S	S	M	M	M	M	M	M	M	M	L	M
CO-03	S	S	M	M	M	M	M	M	M	M	L	M
CO-04	S	S	M	M	M	M	M	M	M	M	L	M
CO-05	S	M	M	M	M	M	M	M	M	M	L	M

S- Strong, M- Medium, L-Low, N- Not Relevant

UNIT I INTRODUCTION TO ENERGY FROM WASTE:

Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

UNIT II BIOMASS PYROLYSIS: PYROLYSIS:

Types, slow fast – Manufacture of charcoal – Methods -Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III BIOMASS GASIFICATION:

Gasifiers – Fixed bed system – Downdraft and updraft gasifiers –Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT IV BIOMASS COMBUSTION:

Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT V BIOGAS:

Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

TOTAL: 45 HOURS

REFERENCES

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2003.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.